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David Esseni received the Ph.D in Electronic Engineering from the University of Bologna, and since 2015 he has been Professor of Electronics at the University of Udine, Italy. During year 2000 he was a visiting scientist at Bell Labs -Lucent Technologies, Murray Hill (NJ-USA), and in 2013 he spent six months as a visiting professor at the University of Notre Dame (IN, USA). His research interests are mainly focused on the modelling and the design of advanced semiconductor devices, early assessment of emerging nanoelectronic technologies and neuromorphic computing.
D.Esseni is a Fellow of the IEEE EDS Society, and in 2013 was awarded a Fulbright Research Scholar Fellowship.

D. Esseni is co-author of numerous publications in peer-reviewed journals and conferences, of the book ”Nanoscale MOS transistors: Semi-classical transport and applications” (Cambridge University Press, Cambridge (UK), 2011) and of several book-chapters. In particular, he is co-author of more than 40 papers presented at the International Electron Devices Meeting (IEDM), which is the worldwide leading conference for electron devices. He also holds three U.S.A. patents in the field of non-volatile memories and steep slope transistors.
He was the General Chair of the “International Conference on Simulation of Semiconductors Processes and Devices, SISPAD 2019” held in Udine. He is presently co-chair for the track ‘Emerging Computing Devices and Circuits’ of the European Solid-State Device Research Conference, ESSDERC. He is or has been part of the Technical Program Committee for International Electron Devices Meeting, IEDM, (2003-04 and 2015-16), International Reliability Physics Symposium, IRPS, (2007-2010), European Solid-State Device Research Conference, ESSDERC, (since 2006), International Conference on Simulation of Semiconductors Processes and Devices, SISPAD (since 2016). He has been Associate Editor of IEEE Transactions on Electron Devices and is presently editor of Frontiers in Electronics.
David Esseni has been the principal investigator (PI) at the University of Udine for the EU funded projects: BeFerroSynaptic, H2020, GA: 871737 (2020-2023), STEEPER, FP7, GA:257267 (2010-2013), and NANOSIL, FP7-ICT-2007-1 (2008-2011), as well as for the PRIN 2017 project FIVE2D (2017SRYEJH 2020-2024). He was work-package leader for modelling and simulations in the EU funded III-V-MOS project, FP7, GA:619326 (2014-2017), and presently is work-package leader in the BeFerroSynaptic project. In year 2017 he was PI for an exchange a collaboration project between the University of Udine and the Massachusetts Institute of Technology (Boston, USA).
He has also been the PI for industry driven projects funded by NXP Semiconductors (2008-2010) and TSMC (2011-2016).
He has been part of the evaluation Panel of the European Science Foundation for the Graphene Flagship in 2014, and reviewer for the ERC-2022-STG Call in 2022.
He has been the thesis advisor for about 40 students, the supervisor for 12 PhD students (2 current), and has supervised the research activities of several postdocs. All his former students have continued a successful career in research centers, in high technology companies or in the academia.